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Description

[BUMP PROCESS FOR FLIP CHIP PACKAGE]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no.92114347, filed on May 28, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention generally relates to a process for fabricating a flip chip package. More particularly, the present invention relates to a bump process for fabricating a flip chip package.

[0004] Description of the Related Art

[0005] Flip chip bonding technology is a technique for connecting a chip to a carrier. Before the connection, a chip with an active surface having an array of die pads thereon is provided. Thereafter, bumps are formed respectively on the die pads of the chip. The chip is flipped over and

bonded with the carrier such that the die pads of the chip are electrically and structurally connected to the contacts of the carrier via the bumps. Through circuits embedded within the carrier, the chip is able to communicate electrically with an external device. Since flip chip bonding technique is able to produce a flip chip package with a high pin count, a small package area and a short transmission path, flip chip bonding processes are widely adopted in the fabrication of high grade chip packages.

[0006] Figs. 1A through 1H are schematic cross-sectional views showing the steps of forming a convention flip chip package. As shown in Fig. 1A, a chip 102 with an active surface 104 having a plurality of die pads 106 thereon is provided. A passivation layer 108 that exposes a portion of these die pads 106 is formed over the active surface 104 of the chip 102. In addition, a plurality of under bump metallurgy (UBM) layers 110 is formed over various die pads 106. Furthermore, a stress buffer layer (SBL) 112 that exposes various UBM layers 110 is formed over the passivation layer 108. The stress buffer layer (SBL) 112 is fabricated using a material such as benzocyclobutene (BCB).

[0007] As shown in Fig. 1B, a photoresist layer 114 is formed on

the active surface 104 of the chip 102. Thereafter, as shown in Fig. 1C, a plurality of openings 116 is formed on the photoresist layer 114 by performing photo-exposure and chemical development process. The openings 116 expose various under bump metallurgy layers 110 so that the die pads 106 are indirectly exposed.

[0008] As shown in Fig. 1D, a printing process is carried out to fill conductive material into the openings 116. Thereafter, a reflow process is performed so that the conductive material inside the openings 116 is cured to form a plurality of short cylindrical bumps 118. Afterwards, the photoresist layer 114 is removed to expose the sides of the bumps 118 as shown in Fig. 1E. Another reflow process is carried out so that the cylindrical bumps 118 are transformed into spherical bumps 118 as shown in Fig. 1F. Since a chip can be obtained by cutting a wafer, the aforementioned steps can be applied to a wafer prior to cutting the wafer to produce individual chips 102 with bumps 118.

[0009] As shown in Fig. 1G, the chip 102 is flipped over and then the bumps 118 are connected to bump pads 12 on the surface of a substrate 10. Hence, the chip 102 is electrically and structurally connected to the substrate 10 via

the bumps 118. Finally, as shown in Fig. 1H, underfill material is injected to the space between the chip 102 and the substrate 10. Thereafter, the underfill material is cured to form an underfill layer 20. The underfill layer 20 provides to buffer any thermal stress between the chip 102 and the substrate 10 so that cracks at the junction between the bumps 118 and the chip 102 or the substrate 10 is greatly minimized.

[0010] However, the conventional flip chip fabricating process has the following drawbacks: 1. Since a photoresist layer and a photolithographic process are required for fabricating cylindrical bumps, therefore the fabrication cost of the flip chip package is increased. 2. The printing process deployed to form bumps in the openings often produces voids close to the bottom section of the bumps and hence the reliability of the chip connection in the package is poor. 3. The conventional underfill dispensing process frequently produces voids in the underfill layer. Too many voids in the underfill layer may lead to a delamination between the chip and the substrate. Accordingly, the reliability of the package is reduced.

SUMMARY OF INVENTION

[0011] Accordingly, one object of the present invention is to pro-

vide a process of fabricating spherical bumps and an underfill layer on the active surface of a chip inside a flip chip package capable of improving the reliability and reducing the production cost of the flip chip package.

[0012] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a process of fabricating at least a bump and an underfill layer on the active surface of a chip inside a flip chip package. The chip has at a plurality of die pads on the active surface of the chip. First, an adhesive layer is formed over each of the die pads on the active surface of the chip. Thereafter, a plurality of bump balls are scattered on the active surface of the chip. The bump balls are vibratedsuch that only one bump ball adheres to the adhesion layer of each die pad. The remaining unattached bump balls are removed. An underfill material is appliedon the active surface of the chip to encapsulate the attached bump balls except their top surfaces. Accordingly, no photoresist layer and photolithography process are required for fabricating the bump balls, and therefore the fabrication process can be greatly simplified and thus the fabrication cost can be effectively reduced. Further, the reliability of

the flip chip package can also be promoted.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0015] Figs. 1A through 1H are schematic cross-sectional views showing the steps of fabricating a conventional flip chip package.

[0016] Figs. 2A through 2H are schematic cross-sectional views showing the steps of a first bump process for fabricating a flip chip package according to one preferred embodiment of this invention.

[0017] Figs. 3A through 3H are schematic cross-sectional views showing the steps of a second bump process for fabricating a flip chip package according to another preferred embodiment of this invention.

[0018] Fig. 4 is a schematic cross-sectional view showing a flip chip having bump balls thereon as shown in Fig. 2H bonded to a substrate.

[0019] Fig. 5 is a schematic cross-sectional view showing a flip chip having bump balls thereon as shown in Fig. 3H bonded to a substrate.

DETAILED DESCRIPTION

[0020] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0021] Figs. 2A through 2H are schematic cross-sectional views showing the steps of a bump process for fabricating a flip chip package according to one preferred embodiment of this invention. As shown in Fig. 2A, a chip 202 (or a wafer) with an active surface 204 having a plurality of die pads 206 thereon is provided. A passivation layer 208 is formed on the active surface 204 of the chip 202 such that a portion of the die pads 206 is exposed. In addition, an under-bump-metallurgy (UBM) (not shown) layer can be optionally formed on each of the die pads 206 of the

chip 202. Similarly, a stress buffer layer (SBL) (not shown) can be optionally formed over the passivation layer 208. As the process of forming under-bump-metallurgy layers and the stress buffer layer has been already described with reference to Fig. 1A, and therefore the detailed description thereof is omitted.

[0022] As shown in Fig. 2B, an adhesive layer 210 is formed on the surface of each die pads 206. The adhesive layer 210 as a sticky film is preferably comprised of a material that has gluing properties at room temperature, examples of such materials include, but not limited to, an organic surface preservation (OSP) or a flux.

[0023] As shown in Fig. 2C, a large number of bump balls 212 is scattered over the active surface 204 of the chip 202 so that the bump balls 212 are roughly evenly distributed over the active surface 204. In this embodiment, the bump balls 212 are fabricated from a solder material, for example.

[0024] As shown in Fig. 2D, the bump balls 212 are vibrated mechanically using an instrument such as an ultrasonic vibrator. The vibration moves the bump balls 212 on the active surface 204 of the chip 202. With the bump balls 212 set into motion on the active surface 204, one bump

ball 212 will eventually adhere to each adhesive layer 210 as the area of each adhesion layer 210 is designed to catch only one bump ball 212.

[0025] As shown in Fig. 2E, a vacuum suction process can be used to remove all the non-attached bump balls 212 from the surface of the chip 202. The bump balls 212 remaining on the adhesive layer 210 ultimately become the bumps for flip chip connection.

[0026] In this embodiment, a reflow process is performed as shown in Fig. 2F. Within the reflow operation, the bump balls 212 are not only firmly bonded to the respective die pads 206 but also flattened out a little to produce a squashed profile. Furthermore, a coining process may be carried out to planarize the top end of the bump balls 212 so as to improve the degree of co-planarity.

[0027] As shown in Fig. 2G, a coating operation is carried out to form a layer of underfill material over the active surface 204 of the chip 202 surrounding the bump balls 212. Thereafter, the underfill material is semi-cured to form an underfill layer 214.

[0028] Since the underfill layer will encapsulate all of the bump balls 212, therefore a polishing operation is carried out to remove a portion of the underfill layer 214 and to expose

a top surface ofeach the bump ball 212 as shown in Fig. 2H. To provide a larger contact area, the polishing operation can also be used to remove a top portion of the bump balls 212 so that a larger contact area and planar surface is formed at the top surface of the bump balls 212. Similarly, to provide a larger junction area, the top surface of the bump balls 212 may be slightly flattened out by applying pressure during the reflow process. Since the top surface of the bump balls 212 has been flattened out, the polishing operation only need to remove the underfill layer 214 and expose the flat top surface of the bump balls 212. After the polishing operation, an additional cleaning operation can be carried out to remove any residual underfill material from the top surface of the bump balls 212 to provide a clean metallic bonding surface. Furthermore, flux material can be applied to the exposed surface of the bump balls 212 to protect the bump balls 212 as well as to increase the bondability of the bump balls 212.

[0029] Because individual chips can be obtained by cutting a fabricated wafer, it is possible to perform all the aforementioned steps on the wafer before cutting the wafer. In other words, all the process steps of forming the bump

balls 212 and the underfill layer 214 can be carried out on a wafer before dicing the wafer to form individual chips 202.

[0030] Fig. 4 is a schematic cross-sectional view showing a flip chip having bump balls thereon as shown in Fig. 2H bonded to a substrate. Since the underfill layer 214 has already formed on the active surface 204 of the chip 202, the bump balls 212 can respectively connect with the bonding pads 14 on the substrate 10 after flipping over the chip 202. In addition, the underfill layer 214 is cured so that the underfill material is able to fill the space bounded by the chip 202, the substrate 10 and the bump balls 212 without carrying out a specific underfill material filling process. This arrangement lowers the probability of producing voids in the underfill layer 214, thereby increasing the reliability of the chip 202 inside the flip chip package.

[0031] Figs. 3A through 3H are schematic cross-sectional views showing the steps of a bump process for fabricating a flip chip package according to another one preferred embodiment of this invention. As shown in Fig. 3A, a chip 302 with an active surface 304 having a plurality of die pads 306 thereon is provided. A passivation layer 308 is

formed on the active surface 304 of the chip 302, wherein a portion of the die pads 306 is exposed. In addition, an under-bump-metallurgy (UBM) (not shown) layer can be optionally formed on each of the die pads 306 of the chip 302. Similarly, a stress buffer layer (SBL) (not shown) can be optionally formed over the passivation layer 308. As the process of forming under-bump-metallurgy layer and the stress buffer layer has been already described in detail with reference to Fig. 1A, therefore a detailed description thereof is omitted.

[0032] As shown in Fig. 3B, an adhesive layer 310 is formed on the exposed surface of the die pads 306. The adhesive layer 310 is preferably comprised of a material that has gluing properties at soldering temperature including, for example, a solder material, a low melting point metal or a low melting point alloy.

[0033] As shown in Fig. 3C, a large number of bump balls 312 is scattered over the active surface 304 of the chip 302 so that the bump balls 312 are roughly evenly distributed over the active surface 304. In this embodiment, the bump balls 312 are comprised of a high melting point metal or a high melting point alloy, for example. These bump balls 312 have a melting point higher than the ad-

hesive layer 310.

[0034] As shown in Fig. 3D, the bump balls 312 are vibrated mechanically using an instrument such as an ultrasonic vibrator. The vibration moves the loose bump balls 312 on the active surface 304 of the chip 302. In the meantime, a reflow process is carried out on the adhesive layer 310 so that the adhesive layer 310 melts under the soldering temperature. However, the bump balls 312 remain in a solid state due to its higher melting point. The melted adhesion layer 310 has great cohesive strength with the solid bump balls 312. Hence, after the reflow process, one bump ball 312 will be attached to the adhesion layer 310 on each die pad 306. In other words, the bump balls 312 are respectively connected to die pads 306 via the adhesion layers 310.

[0035] As shown in Fig. 3E, a vacuum suction process can be used to remove all the non-attached bump balls 312 from the surface of the chip 302. The bump balls 312 remaining on the adhesive layer 310 ultimately become the bumps for flip chip connection.

[0036] As shown in Fig. 3F, a coating operation is carried out to form a layer of underfill material over the active surface 304 of the chip 302 to encapsulate the bump balls 312.

Thereafter, the underfill material is semi-cured to form an underfill layer 314.

[0037] As shown in Fig. 3G, a polishing operation, for example, is carried out to remove a portion of the underfill layer 314 and to expose a top surface of the bump balls 312. Moreover, the polishing operation can also be used to remove a portion of the top surface of the bump balls 312 so that a larger and flatter contact area is formed at the top surface of the bump balls 312.

[0038] As shown in Fig. 3H, a surface finish layer 316 for increasing the bonding strength with an external contact is formed on the exposed surface of the bump balls 312. The surface finish layer 316 is a nickel-gold (Ni/Au) layer or a solder layer, for example. However, the surface finish layer 316 can also be an organic surface preservation (OSP) layer for preventing the surface of the bump balls 312 from oxidation.

[0039] Because individual chips can be obtained by cutting a fabricated wafer, it is possible to perform all the aforementioned steps on the wafer before cutting the wafer. In other words, all the process steps of forming the bump balls 312 and the underfill layer 314 can be carried out on a wafer before dicing the wafer to form individual chips

302.

[0040] Fig. 5 is a schematic cross-sectional view showing a flip chip having bump balls thereon as shown in Fig. 3H bonded to a substrate. Since the underfill layer 314 has already formed on the active surface 304 of the chip 302, the bump balls 312 can respectively connect with the bonding pads 14 on the substrate 10 after flipping over the chip 302. In addition, the underfill layer 314 is cured so that the underfill material is able to fill the space bounded by the chip 302, the substrate 10 and the bump balls 312 without carrying out a specific underfill material filling process. This arrangement lowers the probability of producing voids in the underfill layer 314, thereby increasing the reliability of the chip 302 inside the flip chip package.

[0041] In the first embodiment of this invention, solder bump balls as well as an underfill layer are formed on the active surface of a chip. An adhesive material (for example, flux) with adhesive properties at room temperature is used to position and attach a bump ball to each die pad. Finally, an underfill material is formed over the active surface of the chip to encapsulate the bump balls but to expose a top surface of the bump balls.

[0042] Similarly, in the second embodiment of this invention, metal bump balls as well as an underfill layer are formed on the active surface of a chip. The bump balls are fabricated using a high melting point metal (or a high melting point alloy). Using an adhesive material (for example, a solder material) having adhesive properties at the soldering temperature to form an adhesive layer, the bump balls are positioned and attached to the adhesive layer when the temperature is raised to the melting point temperature of the solder material. Thereafter, an underfill material is formed over the active surface of the chip to encapsulate the bump balls but to expose a top surface of the bump balls.

[0043] In summary, the bump process for fabricating a flip chip package includes the following advantages: 1. Bump balls are used to form the bumps in the flip chip package. Since the bottom section of the bump balls for connecting with the die pads of the chip no longer has any voids, the reliability of the flip chip package is improved. 2. A simple mechanical vibrator is used to vibrate bump balls into position on the adhesion layer for forming the bump balls instead of carrying out a complicated and time-consuming photolithographic process. Hence, production

cost of the flip chip package is greatly reduced. 3. Underfill material is applied over the active surface of the chip to encapsulate the bump balls. Hence, the underfill material can be directly used to fill up the space bounded by the chip and the chip carrier when the chip is flipped over and bonded with the chip carrier (or main board). Since there is no need to carry out a conventional underfill filling process, overall reliability of the flip chip package is improved. 4. The bump process can be applied to fabricate a chip scale package (CSP). The chip is capable of connecting to a system circuit board (for example, a main board) via the bump balls in a direct chip attaching (DCA) method.

[0044] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.